Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) In a multiprocessor digital signal processing system, the combination comprising;

a plurality of processors; and

a single coder/decoder having a digital/analog conversion channel time division multiplexed among, and an analog/digital conversion channel concurrently coupled to, said plurality of ~~the multiple~~ processors ~~thereof~~.

2. (currently amended) In a multiprocessor digital signal processing system according to claim 1, further comprising: ~~The combination of Claim 1 including~~

means for individually selecting input digital signals and analog signals for digital/analog conversion and analog/digital conversion, respectively; and

means for ~~, and~~ assigning which of ~~the multiple~~ said plurality of processors ~~in the system couples the output~~ is coupled to ~~the~~ said digital/analog conversion channel.

3. (currently amended) A digital signal processing system comprising:

a single coder/decoder having a digital signal input, ~~and~~ an analog signal inputs, ~~and~~ a digital/analog conversion channel, and an analog/digital conversion channels;

a first source of an analog input signals coupled to said analog signal input of said single coder/decoder;

a second source of digital input signals coupled to said digital signal input of said single coder/decoder;

a first plurality of ~~signal~~ processors ~~coupled between said source of digital input signals and~~ multiplexed to said digital signal input of said coder/decoder; and

means for time division multiplexing said first plurality of processors to said digital signal input ~~digital/analog conversion channel~~ of said single coder/decoder;

whereby ~~digital-to-analog converted signals are time division multiplexed at said analog output of said coder/decoder, and~~ an analog-to-digital converted signals ~~are~~ is concurrently accessible to all of said first plurality of processors ~~at such digital output of said coder/decoder~~.

4. (currently amended) The digital signal processing system according to claim 3, further comprising: ~~of Claim 3 also including~~

a second plurality of ~~signal~~ processors coupled to ~~said~~ a digital output of said single coder/decoder for operating on said analog-to-digital converted signals.

5. (currently amended) The digital signal processing system according to claim ~~of Claim~~ 4, wherein each of said first plurality of ~~signal~~ processors comprise: ~~also include~~

a ~~plurality of registers~~ register to buffer digital signal data for use by said digital signal input of said single coder/decoder.

6. (currently amended) The digital signal processing system according to claim 1, further comprising: ~~of Claim 5 wherein said second plurality of signal processors also include~~

a plurality of registers to buffer digital signal data from said single coder/decoder to each of said first plurality of processors.

7. (currently amended) The digital signal processing system according to claim 6, further comprising: ~~of Claim 6 wherein said~~

means ~~includes a multiprocessor~~ for individually selecting time slots for digital signals ~~and analog signals~~ from each of said first plurality of processors to access said digital signal input of ~~and second sources for digital-to-analog and analog-to-digital conversions, respectively, by~~ said coder/decoder.